2.2.1 The institution assesses the learning levels of the students and organizes special programs for advanced learners and slow learners

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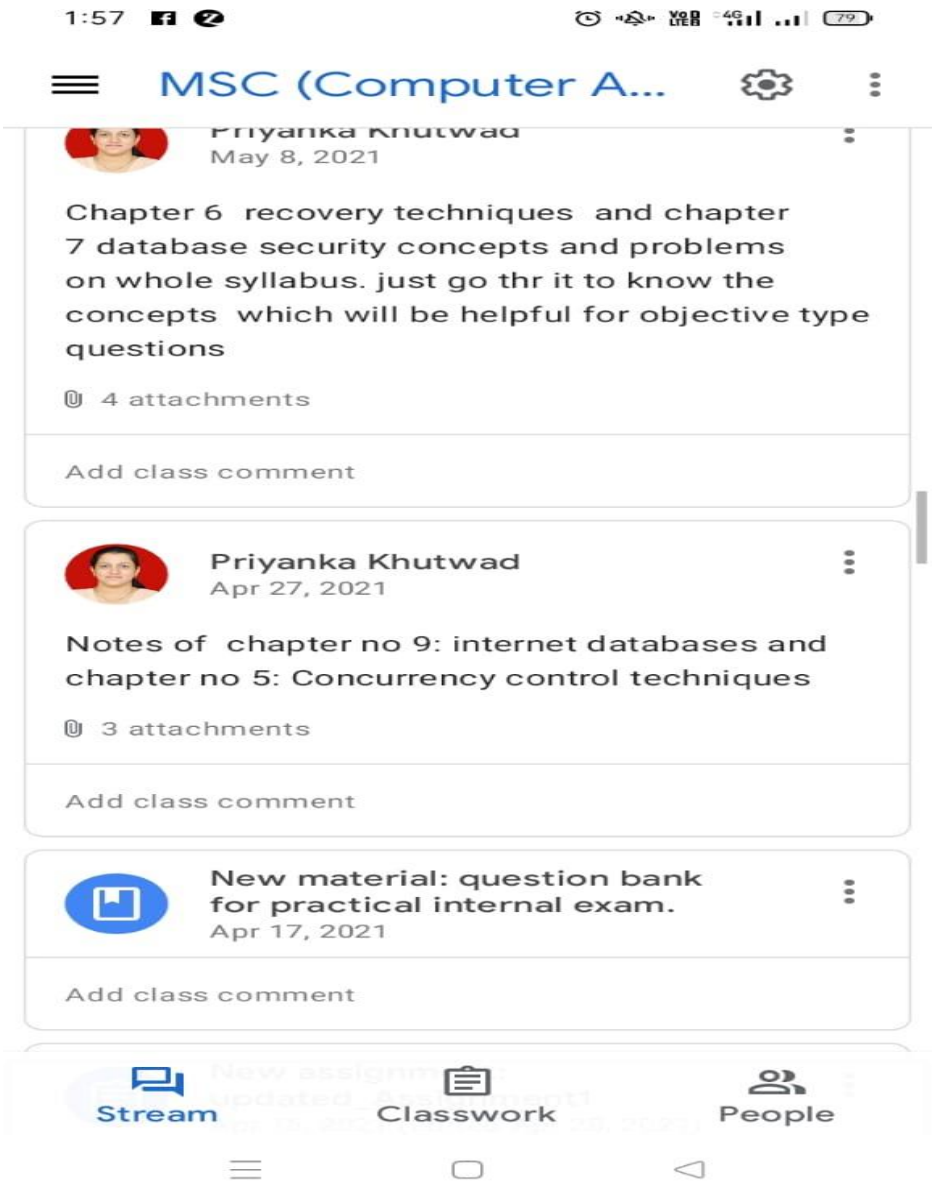

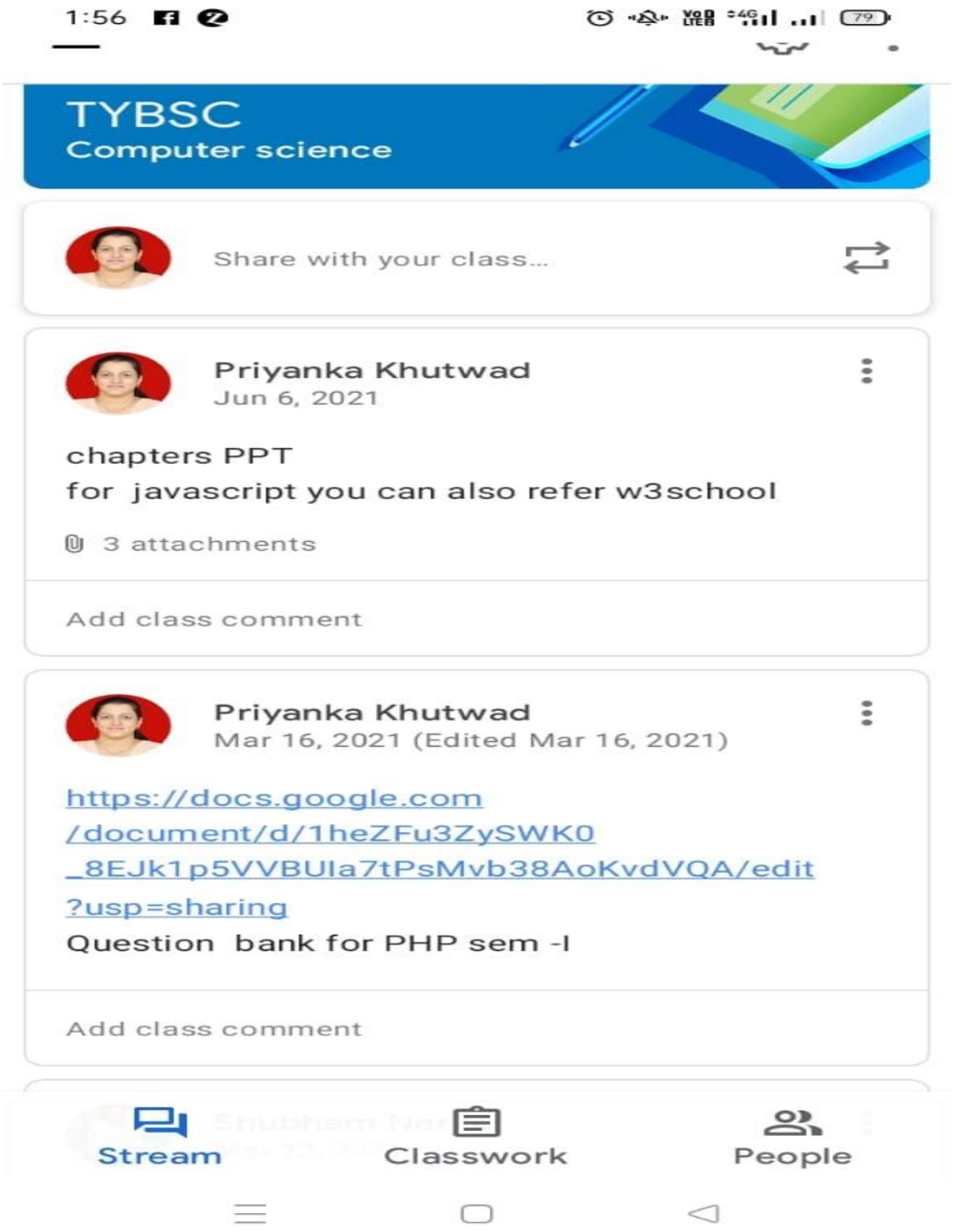
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question bank for practical internal exam.

Dear students
Instructions for practical internal exam.
Dear Students
Please Note:
Subject : Web Technology
Date:17/04/2021
1. Exam Time : 6:00 pm to 6:30 pm
2. Exam will be conducted with Google Form platform.
3. Please enter full Name, valid email (compulsory).
4 . Read the questions carefully and submit answers accordingly.
5. Link will be shared five minutes before the exam.
6. Link will be closed at 6:30 pm sharp.
7. Attendance is compulsory.
8.total 30 marks.

**ALL THE BEST

You can study from this question bank. and assignment2(xml).

Attachments

question_Bank...docx

assignment2.docx

P. V. G's College of Science Pune 09

Class : S. Y. B.Sc.(Comp Sci.) Year 2020-21

Question Bank for Internal Examination I

1) The transformation matrix T represents……

$[T] = \begin{bmatrix} 1 & 0 \\ 0 & 5 \end{bmatrix}$

a) Shearing in Y direction
b) Scaling in X direction only
c) Scaling in Y direction only
d) Rotation about origin

2) The transformation matrix T represents……

$[T] = \begin{bmatrix} 1 & 5 \\ 3 & 1 \end{bmatrix}$

a) Combined transformation
b) Shearing in X direction proportional to y coordinate by 5 and in Y direction proportional to x coordinate by 3 units
c) Scaling in X and Y directions by 3 and 5 units respectively
d) Shearing in X direction proportional to y coordinate by 3 and in Y direction proportional to x coordinate by 5 units

3) Transformation matrix of Rotation about origin through 45^o is

a) $\begin{bmatrix} \mathbf{1/\sqrt{2}} & \mathbf{1/\sqrt{2}} \\ \mathbf{-1/\sqrt{2}} & \mathbf{1/\sqrt{2}} \end{bmatrix}$

b) $\begin{bmatrix} 1/\sqrt{2} & -1/\sqrt{2} \\ 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$

c) $\begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} \\ 1/\sqrt{2} & -1/\sqrt{2} \end{bmatrix}$

d) $\begin{bmatrix} -1/\sqrt{2} & 1/\sqrt{2} \\ 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$

4) The transformation matrix T represents……

$[T] = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$

a) Reflection about X axis
b) Reflection about Y axis
c) Reflection through origin
d) Reflection about line y=x

5) Translation of point P[1 3 1] in X and Y directions by units 2 and 4 respectively transforms it into P' = ……..
   a) [2 4 7]
   b) [3 7 1]
   c) [1 3 7]
   d) [7 3 1]

6) Coordinates of point P[2 8] in homogeneous coordinate system are…..
   a) [10 40 1]
   b) [2 8 10]
   c) [2 8 0]
   d) [2 8 1]

7) Coordinates of point in homogeneous coordinate systemP[2 4 8] are transformed in physical coordinate system then P' = …..
   a) [2 4]
   b) [1 2]
   c) [0.25 0.5]
   d) [0.5 0.25]

8) Scaling of P[0 0] in X direction by 10 units is
   a) [0 0]
   b) [10 10]
   c) [10 0]
   d) [0 10]

9) Reflection of P[3 1] about Y axis is P' = ……
   a) [1 3]
   b) [-3 1]
   c) [3 -1]
   d) [-3 -1]

10) If unit circle $x^2 + y^2 = 1$ scaled in X direction b 2 units then it will be Converted into……
   a) Circle
   b) Rectangle

c) Triangle
d) Ellipse

11) If scaling in X direction by 5 units is applied on line segment A(1 4) B[3 2] then midpoint of transformed line segment A'B' is

a) [10 3]
b) [10 15]
c) [15 10]
d) [3 10]

12) If line l : y = 2x +5 is translated by 2 in direction to get new line l'
Then slope of l' = ……

a) 5/2
b) 2/5
c) 2
d) 4

13) Find slope of transformed line if following transformation T is applied on line l : y = 2x +3 where [T] = $\begin{bmatrix}1 & 1\\0 & 2\end{bmatrix}$

a) **5**
b) 2
c) 3
d) 4

14) Find y intercept of transformed line if following transformation T Is applied on line l : y = x +1 where [T] = $\begin{bmatrix}0 & 1\\1 & 1\end{bmatrix}$

a) 1/2
b) **-1/2**
c) 1
d) -2

15) If transformation T is applied on lines on l1 and l2 to get new lines l1' and l2' , p[2 1] is point of intersection of l1 and l2 then point of intersection of new lines is ……

[T] = $\begin{bmatrix}1 & 2\\3 & 1\end{bmatrix}$

a) [2 1]
b) [-5 5]
c) [-2 1]
d) [5 5]

16) Sequence of matrices in concatenated transformation of rotation About point A(4 , 3) is
   a) Translation, rotation , (Translation)$^{-1}$
   b) Rotation, translation , (Rotation)$^{-1}$
   c) Translation, rotation , Reflection
   d) Translation, reflection , rotation

17) If transformation T is applied on lines l1 : y = 4x +1 and l2 : y = 4x-2 Then transformed lines have slopes m1 and m2….. (where [T] = $\begin{bmatrix}1 & 1\\0 & 2\end{bmatrix}$)
   a) 2, 4
   b) **4, 4**
   c) 3, 1
   d) 3 3

18) Units of translation in first matrix required for reflection through line x=2 are…
   a) 2, 0
   b) 0, 2
   c) -2, 0
   d) 2, 2

19) Units of translation in first matrix required for reflection through line y = -3 are…
   a) 0, 3
   b) -3, 0
   c) 3, 0
   d) 3, 3

20) Total number of matrices required in two dimensional transformation for general reflection are……
   a) 3
   b) 5
   c) 6
   d) 4

21) Total number of matrices required in two dimensional transformation for reflection through line y = mx are……
   a) 5
   b) 4
   c) 3
   d) 7

22) Sequence of matrices in concatenated transformation of

Reflection through line y = mx is ……

a) **Rotation , reflection, $(\text{Rotation})^{-1}$**
b) Rotation , reflection, Scaling
c) Rotation , translation, $(\text{Rotation})^{-1}$
d) Rotation , reflection, $(\text{Translation})^{-1}$

23) If transformation T is applied on an object X having area A then Area of transformed object is ……..

a) Abs(det(T))
b) Abs(det(T) * A)
c) A
d) Abs(A)

24) Appling transformation T line segment can be transformed into

a) Circle
b) Ellipse
c) Triangle
d) Line segment only

25) Inverse of following transformation T where

$$[T] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 2 & 1 \end{bmatrix} \text{ is}$$

a) $\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 1/2 & 1 \end{bmatrix}$

b) $\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & -1/2 & 1 \end{bmatrix}$

c) $\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ -1 & -2 & -1 \end{bmatrix}$

d) $\begin{bmatrix} \mathbf{1} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{1} & \mathbf{0} \\ \mathbf{-1} & \mathbf{-2} & \mathbf{1} \end{bmatrix}$

26) Inverse of following transformation T is

$$[T] = \begin{bmatrix} \cos(\phi) & \sin(\phi \\ -\sin(\phi & \cos(\phi \end{bmatrix} \text{ is}$$

a) $\begin{bmatrix} \boldsymbol{\cos(\phi)} & \boldsymbol{-\sin(\phi} \\ \boldsymbol{\sin(\phi} & \boldsymbol{\cos(\phi} \end{bmatrix}$

b) $\begin{bmatrix} \cos(\phi) & \sin(\phi \\ -\sin(\phi & -\cos(\phi \end{bmatrix}$

c) $\begin{bmatrix} \cos(\phi) & -\sin(\phi \\ -\sin(\phi & \cos(\phi \end{bmatrix}$

d) $\begin{bmatrix} -\cos(\phi) & \sin(\phi \\ -\sin(\phi & \cos(\phi \end{bmatrix}$

27) If transformation T is applied on circle to get new object X whose Area is 144$\boldsymbol{\pi}$sq.units and [T] = $\begin{bmatrix} 2 & -1 \\ 5 & 3 \end{bmatrix}$ then radius of circle is……

a) 4 units
b) 8 units
c) 1 unit.
d) 16 units

Question Bank (MCQ & Descriptive)
Sem. :- II Class :- F. Y. B. Sc. (Comp. Sci.)
Subject :- Basics of Computer Organization (Electronics - II)

Q. 1 Multiple Choice Questions

1. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
a) Low input voltages
b) Synchronous operation
c) Gate impedance
d) Cross coupling
2. When both inputs of a J-K flip-flop 1 and without clock cycle, the output will _____
a) Be invalid
b) Change
c) Not change
d) Toggle
3. Which of the following is correct for a gated D-type flip-flop?
a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
b) The output complement follows the input when enabled
c) Only one of the inputs can be HIGH at a time
d) The output toggles if one of the inputs is held HIGH
4. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates
5. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops
6. Whose operations are more faster among the following?
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops
7. The basic latch consists of _____

a) Two inverters
b) Two comparators
c) Two amplifiers
d) Two adders
8. In S-R flip-flop, if Q = 0 the output is said to be _____
a) Set
b) Reset
c) Previous state
d) Current state
9. The output of latches will remain in set/reset until _____
a) The trigger pulse is given to change the state
b) Any pulse given to go into previous state
c) They don't get any pulse more
d) The pulse is edge-triggered
10. What is a trigger pulse?
a) A pulse that starts a cycle of operation
b) A pulse that reverses the cycle of operation
c) A pulse that prevents a cycle of operation
d) A pulse that enhances a cycle of operation
11. The circuits of NOR based S-R latch classified as asynchronous sequential circuits, why?
a) Because of inverted outputs
b) Because of triggering functionality
c) Because of cross-coupled connection
d) Because of inverted outputs & triggering functionality
12. Combinational circuit have Memory Element to store data.
a) True
b) False
13. Latches are classified as Synchronous & Asynchronous latch.
a) True
b) False
14. D flip flop eliminates the --------- combinations of SR inputs, therefore it holds information available on its input.
a) Different
b) Same
c) None of above
15. In the level Triggered "T" Flip Flop output Toggles after every --------- time.
a) Propagation delay
b) Input delay
c) T=1
d) None of above
16. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
a) Tristate

b) End around
c) Universal
d) Conversion
17. How can parallel data be taken out of a shift register simultaneously?
a) Use the Q output of the first FF
b) Use the Q output of the last FF
c) Tie all of the Q outputs together
d) Use the Q output of each FF
18. The group of bits 1111 is serially shifted (right-most bit first) into a 4-bit parallel output shift register with an initial state 0000. After three clock pulses, the register contains _____
a) 1100
b) 1001
c) 1110
d) 1111
19. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)
a) 1100
b) 0011
c) 0000
d) 1111
20. ------ no. of clock pulses needs to shift in 4 bit data serially & shift out parallel.
a) 7
b) 4
c) 5
d) 3
21. In digital logic, a counter is a device which _____
a) Counts the number of outputs
b) Stores the number of times a particular event or process has occurred
c) Stores the number of times a clock pulse rises and falls
d) Counts the number of inputs
22. A counter circuit is usually constructed of _____
a) A number of latches connected in cascade form
b) A number of NAND gates connected in cascade form
c) A number of flip-flops connected in cascade
d) A number of NOR gates connected in cascade form
23. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
a) 0 to 2n
b) 0 to 2n + 1
c) 0 to 2n – 1
d) 0 to 2n+1/2
24. Ripple counters are also called _____

a) SSI counters
b) Asynchronous counters
c) Synchronous counters
d) VLSI counters
25. BCD counter is also known as _____
a) Parallel counter
b) Decade counter
c) Synchronous counter
d) VLSI counter
26. The type of register, in which we have access only to leftmost or rightmost flip-flop is.
a) shift left & shift right register
b) serial in & serial out shift register
c) serial in &parallel out shift register
d) parallel in & serial out shift register
27. Which of the following statement are true regarding a synchronous up/down counter?
a) It can count in any direction but direction can't be changed once counting has started
b) The direction can be changed midway, but the counter has to be reset before that can be done
c) The counter can be reversed at any moment, no strings attached
d) The direction cannot be changed midway, and when changed the counter has to be reset first
28. The delay problems encountered with asynchronous counters are removed with synchronous counters because the:
a) Input clock pulses are applied simultaneously to each stage
b) Input clock pulses are not used to activate any of the counter stages
c) Input clock pulses are not used to activate any of the counter stages
d) Input clock pulses are applied only to the first and last stages
29. Which is not an example of a truncated modulus counter?
a) 8
b) 5
c) 6
d) 15
30. _____ is the basic memory unit in digital electronics and hold 1-bit of data.
a) Encoder
b) NAND gate
c) EX-OR gate
d) Flip-Flop
31. A 32-bit address bus allows access to a memory of capacity
a) 64 Mb
b) 16 Mb
c) 1 Gb
d) 4 Gb

32. The system bus is made up of
a) data bus
b) data bus and address bus
c) data bus and control bus
d) data bus, control bus and address bus
33. Which of the following data transfer mode takes relatively more time?
a) DMA
b) interrupt initiated I/O
c) programmed I/O
d) Isolated I/O
34. Which of the following holds data and processing instructions temporarily unit the CPU needs it?
a) ROM
b) control unit
c) main memory
d) coprocessor chips
35. Which of the following affects processing power?
a) data bus capacity
b) addressing scheme
c) clock speed
d) all of the above
36. Both the arithmetic logic unit (ALU) and control selection of CPU employ special purpose storage locations called
a) decoders
b) buffers
c) multiplexer
d) registers
37. If the width of data bus is 16, ----- is the largest no. data bus can carry.
a) 256
b) 1KB
c) 65535
d) 65536
38. Input unit receives data from input device & decodes into -------- language, and then load it to CPU.
a) 1 & 0
b) Machine
c) High
d) Assembly
39. The combined value of a binary selection inputs specifies the ------- word.
a) data
b) address
c) control
d) none of above
40. ---- register holds the topmost address on stack.

a) program counter
b) stack pointer
c) address register
d) none of the above
41. Stack pointer is incremented after PUSH operation in Memory Stack.
a) True
b) False
42. I/O interface unit is required, due to the difference in the mode of operation of both peripheral devices and CPU.
a) True
b) False
43. Transferring data under programmed I/O requires --------- monitoring of the peripherals by the CPU.
a) frequent
b) Interrupt based
c) constant
d) none of above
44. The stack is useful for
a) storing the register status of the processor
b) temporary storage of data
c) storing contents of registers temporarily inside the CPU
d) all of the mentioned
45. The method which offers higher speeds of I/O transfers is _____
a) Interrupts
b) Memory mapping
c) Program-controlled I/O
d) DMA
46. What is true about memory unit?
a) A memory unit is the collection of storage units or devices together.
b) The memory unit stores the binary information in the form of bits.
c) Both A and B
d) None of the above
47. Auxiliary memory access time is generally _____ times that of the main memory
a) 10
b) 100
c) 1000
d) 10000
48. What is the formula for Hit Ratio?
a) Hit/(Hit + Miss)
b) Miss/(Hit + Miss)
c) (Hit + Miss)/Miss
d) (Hit + Miss)/Hit
49. The fastest data access is provided using _____
a) Cache

b) DRAM's
c) SRAM's
d) Registers
50. Which of the following is true?
a) To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.
b) If we use the flash drives instead of the hard disks, then the secondary storage can go above primary memory in the hierarchy.
c) In the memory hierarchy, as the speed of operation increases the memory size also increases.
d) Both A and C
51. Cache Memory is implemented using the DRAM chips.
a) True
b) False
52. In _____ mapping, the data can be mapped anywhere in the Cache Memory.
a) Associative
b) Direct
c) Set Associative
d) Indirect
53. The transfer between CPU and Cache is _____
a) Block transfer
b) Word transfer
c) Set transfer
d) Associative transfer
54. --------- is the time interval between the read/write request and the availability of the data.
a) Execution Time
b) Access Time
c) Instruction Cycle
d) Processing Time
55. When data and code lie in same memory blocks, then the architecture is referred as Harvard architecture.
a) True
b) False
56. Because of virtual memory, the memory can be shared among _____
a) processes
b) threads
c) instructions
d) none of the mentioned
57. Which algorithm chooses the page that has not been used for the longest period of time whenever the page required to be replaced?
a) first in first out algorithm
b) additional reference bit algorithm

c) least recently used algorithm
d) counting based page replacement algorithm
58. Which memory is called separation of user logical memory and physical memory
a) Memory sharing
b)Virtual memory
c)Memory management
d) Memory control
59. Logical address space is smaller than physical address space.
a) True
b) False
60. Vertical memory expansion is modifies the no. of address lines (N) that is memory locations (2N). It expands the --------- of memory.
a) Word length
b) Word capacity
c) Memory capacity
d) None of above

Q. 2. Explain in brief the following questions.

1. Draw & explain working of SR latch using NOR gate with truth table.
2. Note down the difference between combinational & sequential circuit
3. Draw & explain JK flip flop using NAND gate with truth table.
4. Draw logic diagram & truth table for D & T flip flop.
5. Explain the terms Propagation delay, Race-around condition & Toggling.
6. Draw & Explain 4 bit SISO shift register.
7. Draw & Explain 4 bit bidirectional shift register.
8. Explain with suitable diagram 4 bit PISO shift register.
9. With suitable diagram & timing diagram explain asynchronous 3 bit binary down counter.
10. Draw 3 bit binary synchronous up/down counter and its timing diagram.
11. Note down the difference between Synchronous & asynchronous counter.
12. Draw & Explain decade counter using JK flip-flop.
13. With suitable diagram explain 4 bit binary Ring Counter.
14. Draw Universal Shift register.
15. Explain the working of decade counter using IC 7490.
16. Explain with suitable diagram System Bus
17. Explain the operation R3=R1+R2 in register based CPU, with suitable diagram.
18. Explain Register based stack organization.
19. Define Memory Stack & explain with suitable diagram.
20. What is the need of I/O interface? Explain in short concept of I/O interface.
21. Draw & explain DMA controller.
22. What is the difference between Programmed I/O, Interrupt Initiated I/O & DMA?
23. Draw & explain general I/O interface unit.
24. Explain Programmed & Interrupt initiated I/O.
25. Define the following terms Capacity, Hit Rati, Performance, and Cost per bit
26. Explain memory write cycle using suitable timing diagram.

27.Design 64X8 memory using 16X8 memory chips.
28.Explain Direct Cache mapping using suitable example.
29.Explain virtual memory mapping using segmentation.

P.V.G's College of Science, Pune 411009
Class : F.Y.B.Sc. (Computer Science) 2020-21
Assignment 1 Topic Introduction to matrices

1) Define and give an example of each of the following

i. Diagonal matrix

ii. Symmetric matrix

iii. Zero matrix

iv. Identity matrix

v. Upper triangular , lower triangular matrices

vi. Determinant of a matrix vii. Inverse of a matrix

2) If A = 2 3 0 B = 3 4 2 find 2A + 3B, B – A, A – B A

1 2 -1 3 1 6 transpose of A,
Can you find A x B ?

3) If A = 2 0 1 B = 5 2 1

-1 2 3 0 2 -3
2 6 4 1 3 4
Find A2 , A2 + 3B - 4I, Also find AXB and BxA, are they same?

4) If A = 1 3 5 2

0 -1 3 1
5 0 2 2
Perform following row operations successively on A

i. R1 * 2

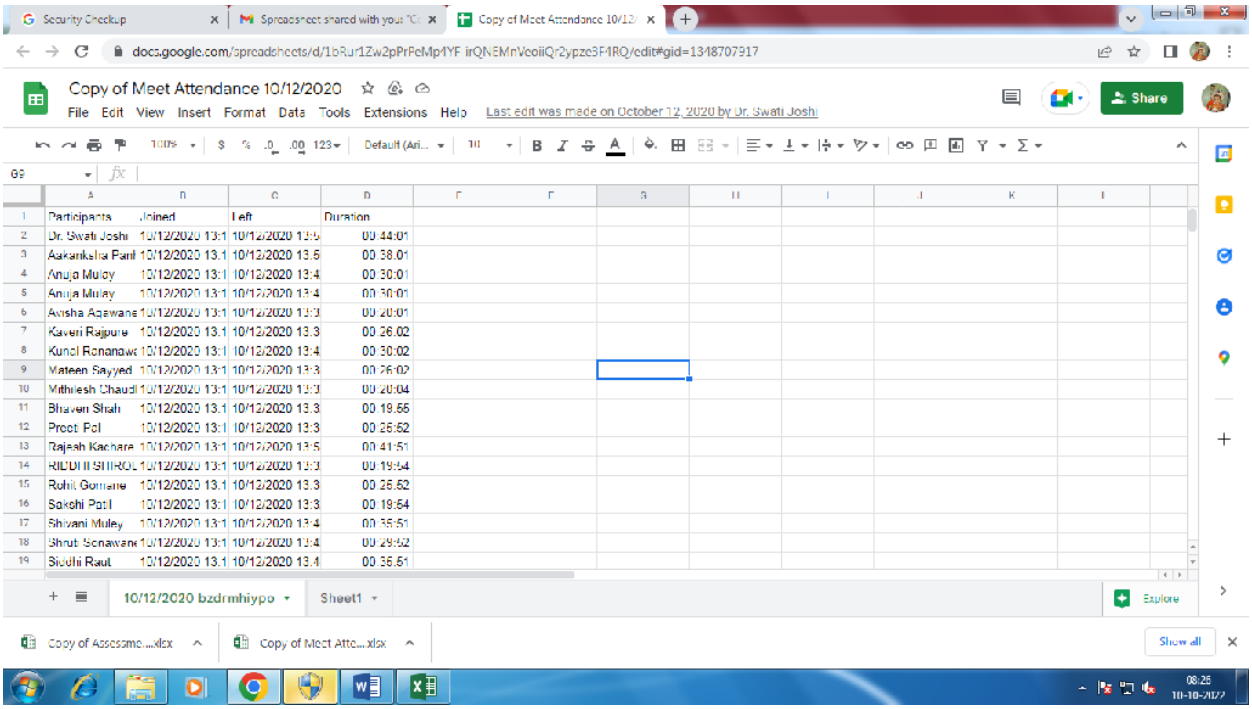
ii. R2 R3 (Exchange of rows)

5) If A = 3 1 9

-1 3 1
0 1 2
Perform following row operations successively on A

i. R1 * 1/3

ii. R2 + R3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Anuja Muley 10/12/2020 13:1 10/12/2020 13:4 00:30:01
Anisha Agawane 10/12/2020 13:1 10/12/2020 13:3 00:20:01
Kaveri Rajpure 10/12/2020 13:1 10/12/2020 13:3 00:26:02
Kunal Rananaw 10/12/2020 13:1 10/12/2020 13:4 00:30:02
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Bhaven Shah 10/12/2020 13:1 10/12/2020 13:3 00:19:56
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